

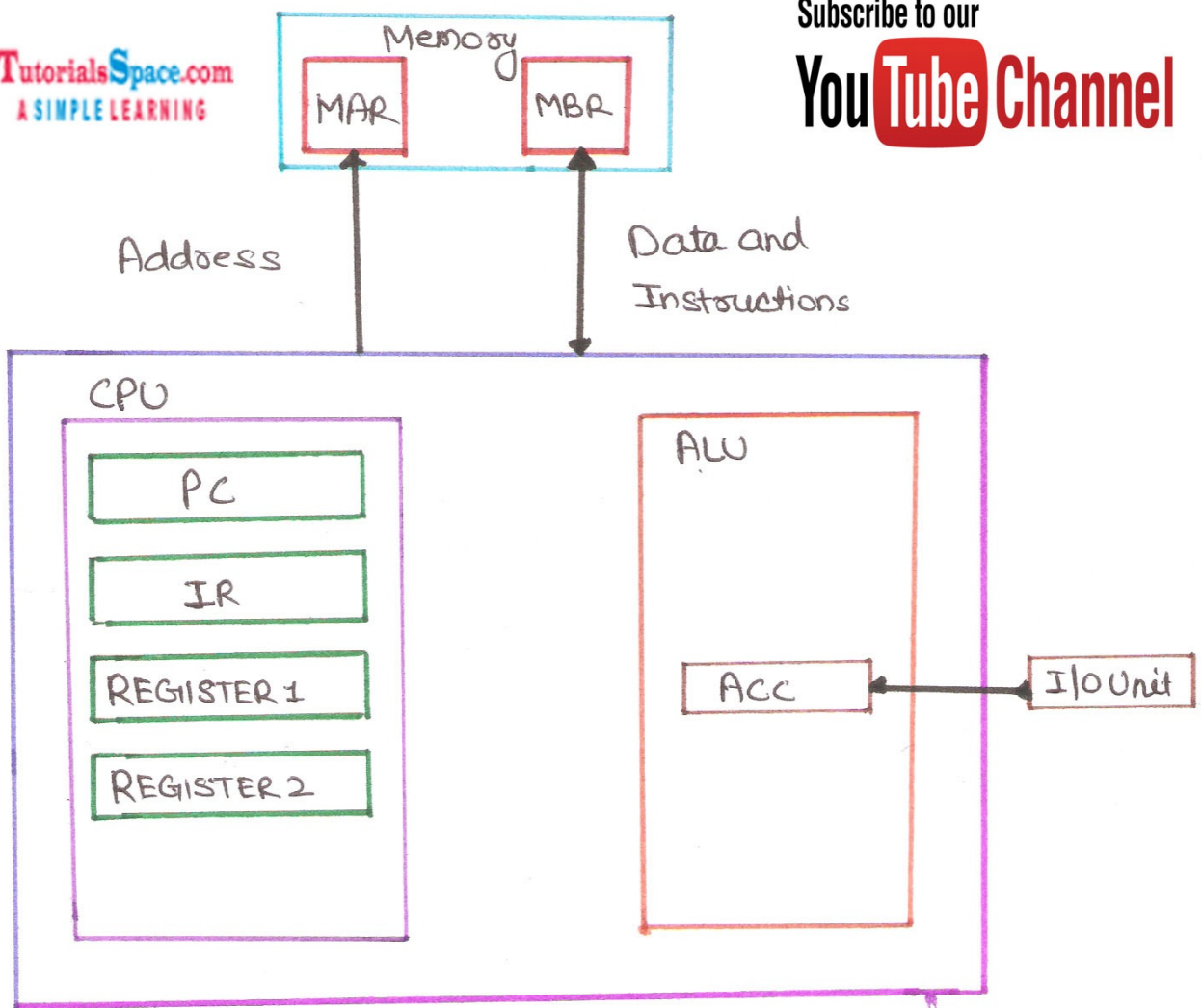
"VON-Neumann MODEL"

A typical uniprocessor Computer System consisting of a memory unit, the ALU, the Control Unit & the I/O unit.

→ The memory unit a single-port device consisting of a "Memory Address Register" MAR and a Memory Buffer Register (MBR) also called a Memory Data Register (MDR)



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'VON-NEUMANN ARCHITECTURE'

→ The Memory Cells are arranged in the form of several memory words, where each word is the unit of data that

Can be Read or Written.

- All the read and write operations on the memory utilize the memory port.
- The ALU performs the arithmetic and logic operations on the data items in the Accumulator (Acc) and/or MBR and typically the Acc retains the results of such operations.
- The Control Unit consists of a Program Counter (PC) that contains the address of the instructions to be fetched and an Instruction Register (IR) into which instructions are fetched from the memory for execution.
- Register 1 & Register 2 used to hold the data and address values during computation.

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→ For simplicity, The I/O Subsystem is shown to input to and output from the ALU System. In practice, the I/O may also occur directly between the memory and I/O Devices without utilizing any processor's registers.

→ In practice, the I/O  and other components of the system are interconnected by a multibus structure on which the data and address flow. Control Unit manages this flow through the use of appropriate control signals.



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This Architecture runs programs in what is known as the Von-Neumann execution Cycle (also called 'Fetch-decode-execute' Cycle), which describes how the machine works.

- The CPU fetches the next program instruction from the memory, using the program counter to determine where the instruction is located.
- Instruction is decoded into a language the ALU can understand.
- Any Data Operands required to execute the instruction are fetched from memory and placed into registers with the CPU i.e. IR.
- The ALU executes the instruction and places the results in registers or memory.



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