

Addressing Mode :- Indexed Addressing Mode



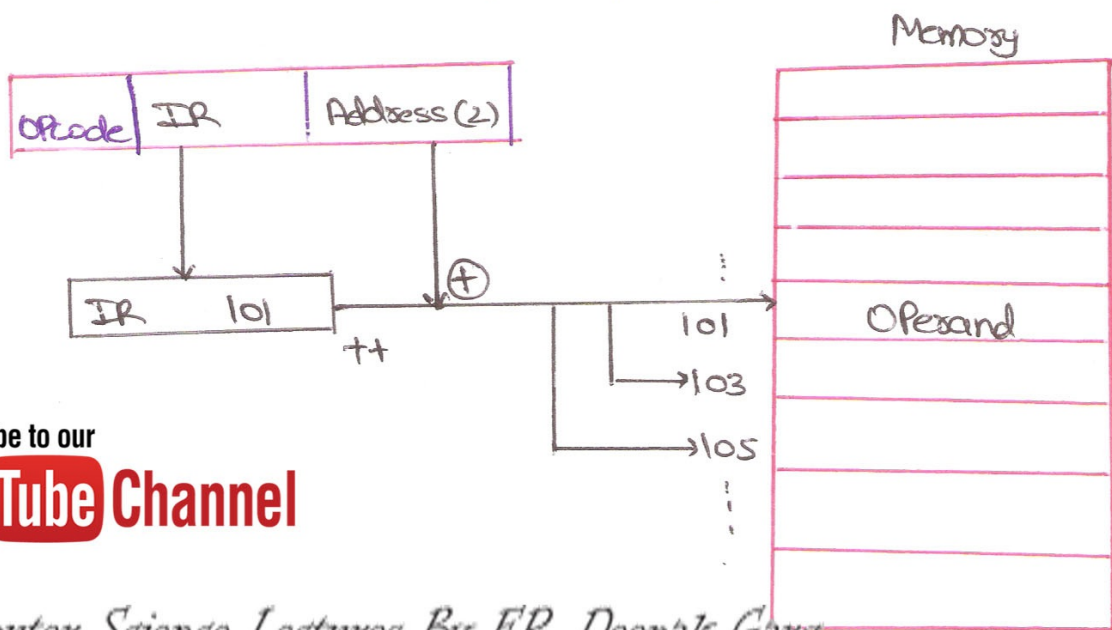
In this Operand field of the instruction Contains an address and an index register, which Contains an offset.

This mode is generally used to address the consecutive locations of memory (which may store the elements of an Array).

The index register is a special CPU Register that contains an index value.

The Contents of the operand field A are taken to be the address of the initial or the reference location (or the first element of the array).

The index register specifies the distance between the starting address and the address of the operand.



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For example, to address of an element $B[i]$ of an array $B[1], B[2], \dots, B[n]$, with each element of the array stored in two consecutive locations, and the starting address of the array is assumed to be 101, the operand field A in the instruction shall contain the number 101 and the index register R will contain the value of the expression $(i-1) \times 2$.

Thus, for the element (first) of the array the index register will contain 0. For addressing 5th element of the array, the $A=101$ where as index Register will contain:-
$$(5-1) \times 2 = 8$$

Therefore, the address of the 5th element of array B is $= 101 + 8 \Rightarrow 109$. In $B[5]$, however, the element will be stored in location 109 and 110. To address any other element of the array, changing the content of the index register will suffice.

Thus, the effective address in this mode is calculated as

$$\begin{aligned} EA &= A + (R) \\ D &= (EA) \\ * DA &= (\text{Direct Address})^* \end{aligned}$$

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